

IN THE CLAIMS

Please cancel claims 8 and 9.

Please amend the claims as follows.

- 1 1. (Currently amended) An apparatus for computer hardware multithreading
2 comprising:
3 a plurality of processors, each processor having hardware support for the
4 capability of executing a plurality of threads;
5 a memory coupled to the plurality of processors; and
6 a thread dispatch mechanism residing in the memory and executed by at least one
7 of the plurality of processors, the thread dispatch mechanism determining which of the
8 plurality of processors are idle, which of the plurality of processors is busy processing a
9 thread but can accept ~~an additional~~ a new thread, and which of the plurality of processors
10 cannot accept ~~an additional~~ the new thread since it is working on a maximum number of
11 threads the processor can execute and, the thread dispatch mechanism dispatching ~~[[a]]~~
12 the new thread to an idle processor, if one exists.
- 1 2. (Currently amended) The apparatus of claim 1 wherein, if none of the plurality of
2 processors is idle and if at least one of the plurality of processors can accept ~~an~~
3 ~~additional~~ the new thread, the thread dispatch mechanism dispatches the new
4 thread to one of the plurality of processors that can accept ~~an additional~~ the new
5 thread.

1 3. (Currently amended) The apparatus of claim 1 wherein, if all of the plurality of
2 processors cannot accept ~~an additional~~ the new thread, the thread dispatch
3 mechanism waits for one of the plurality of processors to complete processing a
4 thread, thereby becoming a processor that can accept ~~an additional~~ the new thread,
5 and then dispatches the thread to the processor that can accept ~~an additional~~ the
6 new thread.

1 4. (Currently amended) A method for dispatching threads in a computer system that
2 includes a plurality of processors that can each support hardware multithreading to
3 execute a plurality of threads, the method comprising the steps of:

4 (1) determining the status of each of the plurality of processors, wherein a
5 processor is idle if not executing any threads, wherein the processor can accept ~~an~~
6 ~~additional~~ a new thread if busy working on one or more threads but has the capacity to
7 process the ~~additional~~ new thread, and wherein the processor cannot accept ~~an additional~~
8 the new thread if busy working on a maximum number of threads the processor can
9 execute; and

10 (2) dispatching ~~[[a]]~~ the new thread to an idle processor, if one exists.

1 5. (Currently amended) The method of claim 4 further comprising the step of:
2 if none of the plurality of processors is idle and if at least one of the plurality of
3 processors can accept ~~an additional~~ the new thread, the thread dispatch mechanism
4 dispatches the new thread to one of the plurality of processors that can accept ~~an~~
5 ~~additional~~ the new thread.

1 6. (Currently amended) The method of claim 4 further comprising the steps of:
2 if all of the plurality of processors cannot accept ~~an additional~~ the new thread, the
3 thread dispatch mechanism waits for one of the plurality of processors to complete
4 processing a thread, thereby becoming a processor that can accept ~~an additional~~ the new
5 thread, and then dispatches the thread to the processor that can accept ~~an additional~~ the
6 new thread.

- 1 7. (Currently Amended) A computer-readable program product comprising:
2 (A) a thread dispatch mechanism that determines which of a plurality of
3 processors in a hardware multithreading, multiprocessor computer system are idle, which
4 of the plurality of processors is busy but can accept ~~an additional~~ a new thread, and which
5 of the plurality of processors cannot accept ~~an additional~~ the new thread since it is
6 working on a maximum number of threads the processor can execute, the thread dispatch
7 mechanism dispatching ~~[[a]]~~ the new thread to an idle processor, if one exists, wherein
8 each processor can execute a plurality of threads; and
9 (B) ~~computer readable signal bearing~~ recordable media bearing the thread dispatch
10 mechanism.
- 1 8. (Cancelled)
- 1 9. (Cancelled)
- 1 10. (Currently Amended) The program product of claim 7 wherein, if none of the
2 plurality of processors is idle and if at least one of the plurality of processors can
3 accept ~~an additional~~ the new thread, the thread dispatch mechanism dispatches the
4 new thread to one of the plurality of processors that can accept ~~an additional~~ the
5 new thread.

- 1 11. (Currently Amended) The program product of claim 7 wherein, if all of the
2 plurality of processors cannot accept ~~an additional~~ the new thread, the thread
3 dispatch mechanism waits for one of the plurality of processors to complete
4 processing a thread, thereby becoming a processor that can accept ~~an additional~~
5 the new thread, and then dispatches the new thread to the processor that can
6 accept ~~an additional~~ the new thread.
- 1 12. (Previously presented) The apparatus of claim 1 wherein all processors are made
2 busy with a first thread before dispatching a second thread to any processor.
- 1 13. (Previously presented) The method of claim 4 wherein all processors are made
2 busy with a first thread before dispatching a second thread to any processor.
- 1 14. (Previously presented) The program product of claim 7 wherein all processors are
2 made busy with a first thread before dispatching a second thread to any processor.